taxial layer **15** is not formed and the second epitaxial layer **13** and the third epitaxial layer **14** are formed to fill up the trenches **12**.

[0080] In a case in which the first epitaxial layer **11** is p-type and the second epitaxial layer **13** and the third epitaxial layer **14** are n-type, in the second epitaxial layer forming step S**3**, the second epitaxial layer **13** can be formed by introducing an n-type dopant gas to the first epitaxial layer **11** and the trenches **12**, at the first dopant gas flow rate, in an atmosphere of approximately 900 to 950° C. In addition, in the third epitaxial layer forming step S**4**, the third epitaxial layer **14** can be formed to fill up the trenches **12**, by introducing an n-type dopant gas at the second dopant gas flow rate that is lower than the first dopant gas flow rate, in an atmosphere of approximately 950 to 1000° C. In this case, the fourth epitaxial layer **15** is not formed and the second epitaxial layer **13** and the third epitaxial layer **14** are formed to fill up the trenches **12**.

[0081] Here, the first dopant amount of the second epitaxial layer **13**, the second dopant amount of the third epitaxial layer **14**, and the third dopant amount of the fourth epitaxial layer **15** are changed by changing the flow rate of the dopant gas of p-type or n-type. In addition, the first dopant amount, the second dopant amount and the third dopant amount are changed by using a plurality of cylinders of different concentrations of the dopant gas of p-type and n-type.

[0082] As described above, in the method of producing a semiconductor substrate of the present invention, the growth temperature can be changed in four levels, not in two or three levels, and the epitaxial layer can be formed inside the trenches **12** while consecutively changing the growth temperature. In addition, although only the growth temperature is changed in the method of producing a semiconductor substrate according to the abovementioned embodiment; however, the present invention is not limited thereto. For example, in the method of producing a semiconductor substrate, the flow rate of at least one of the material gas and the halide gas can be changed.

[0083] Next, a structure of a power MOSFET **2** as a semiconductor device produced using the semiconductor substrate **1** according to the present embodiment is hereinafter described with reference to FIGS. **4** and **5**. FIG. **4** is a partial cross-sectional view schematically showing an embodiment of a semiconductor device according to the present invention. FIG. **5** is a partial cross-sectional view schematically showing another embodiment of a semiconductor device according to the present invention.

[0084] As shown in FIG. **4**, the n-channel power MOSFET **2** includes: the silicon substrate **10**; the first epitaxial layer **11**; the second epitaxial layer **13**; the third epitaxial layer **14**; the fourth epitaxial layer **15**; the fifth epitaxial layer **16**; a source region **17**; an ohmic contact region **18**; and a trench insulated gate electrode **19**.

[0085] The silicon substrate **10** is a drain region. As described above, the first epitaxial layer **11** is an n-type epitaxial layer formed on the silicon substrate **10**.

[0086] The second epitaxial layer **13**, the third epitaxial layer **14** and the fourth epitaxial layer **15** are p-type epitaxial layers. The second epitaxial layer **13**, the third epitaxial layer **14** and the fourth epitaxial layer **15** are formed alternately on the first epitaxial layer **11** and in the trenches **12** that are formed in the first epitaxial layer **11** at predetermined intervals, to be adjacent to the first epitaxial layer **11**.

[0087] The fifth epitaxial layer **16** is a p-type epitaxial layer formed on the fourth epitaxial layer **15**. The fifth epitaxial layer **16** functions as a channel forming layer.

[0088] The fifth epitaxial layer **16** is a p-type epitaxial layer formed on the fourth epitaxial layer **15**. The fifth epitaxial layer **16** functions as a channel forming layer. For example, the fifth epitaxial layer **16** is formed on the fourth epitaxial layer **15**, after flattening of a surface of the fourth epitaxial layer by polishing.

[0089] The n-type source region **17** and the p-type ohmic contact region **18** are formed on the fourth epitaxial layer **15**. The n-type source region **17** is formed by, for example, ion implantation of an n-type dopant to a p-type epitaxial layer. The p-type ohmic contact region **18** is formed by, for example, ion implantation of a p-type dopant.

[0090] The trench insulated gate electrode **19** is formed to penetrate the source region **17**, the fifth epitaxial layer **16**, the fourth epitaxial layer **15**, the third epitaxial layer **14** and a part of the second epitaxial layer **13**. For example, in a step of forming the trench insulated gate electrode **19**, a trench **20** that penetrates the source region **17**, the fifth epitaxial layer **16**, the fourth epitaxial layer **15**, the third epitaxial layer **14** and a part of the second epitaxial layer **13** is formed. On a bottom face and lateral face of the trench **20**, an insulating film **21** is formed by a thermal oxidation method, a CVD method or the like. The trench insulated gate electrode **19** is composed of polycrystal silicon **22** and formed on the insulating film **21** to fill up the trench **20**.

[0091] In the power MOSFET **2** thus obtained, dopant amount in the second epitaxial layer **13**, the third epitaxial layer **14** and the fourth epitaxial layer **15** is constant in the whole area of the second epitaxial layer **13**, the third epitaxial layer **14** and the fourth epitaxial layer **15**. In addition, the power MOSFET **2** shown in FIG. **5** can be obtained by reversing the conductivity types of the components of the power MOSFET **2** shown in FIG. **4**.

[0092] A semiconductor substrate and the method of producing the same according to the present invention have been described above; however, the present invention is not limited thereto. For example, a conductivity type of the silicon substrate **10** and the first epitaxial layer **11** is n-type, and a conductivity type of the second epitaxial layer **13**, the third epitaxial layer **14** and the fourth epitaxial layer **15** is p-type; however, the present invention is not limited thereto. For example, the conductivity type of the silicon substrate **10** and the first epitaxial layer **11** can be p-type, and the conductivity type of the second epitaxial layer **13**, the third epitaxial layer **14** and the fourth epitaxial layer **15** can be n-type.

[0093] In addition, a semiconductor substrate using silicon has been described in the above embodiment; however, the present invention is not limited thereto. For example, a compound semiconductor such as silicon carbide (SiC), gallium arsenide (GaAs) and gallium nitride (GaN) can also be used.

(が 行) EXAMPLES

[0094] Next, the present invention is described further in detail using Examples. Examples are not intended to limit the scope of the present invention.

Example 1

[0095] The semiconductor substrate **1** shown in FIG. **1** was produced by performing the steps S**1** to S**5** described in the above embodiment. A temperature of an atmosphere and a dopant flow rate in formation of the second epitaxial layer **13**,